Claims

What is claimed is:

1. A method of controlling the impedance of a bus in an information handling system (IHS), the method comprising:

providing a board on which a first bus is coupled to a first connector, the first bus exhibiting a bus impedance, the first connector exhibiting a connector impedance which is greater than the bus impedance;

providing a riser card situated in the first connector, the riser card including a second connector exhibiting an impedance approximately equal to the connector impedance of the first connector; and

providing, on the riser card, an interconnect between the first and second connectors, the interconnect exhibiting an impedance sufficiently low to compensate the amount by which the connector impedance exceeds the bus impedance.

2. The method of claim 1 including providing an expansion card situated in the second connector of the riser card.

3. The method of claim 2 wherein the expansion card includes a second bus exhibiting an impedance approximately equal to the bus impedance.

4. The method of claim 1 wherein the first bus is a microstrip transmission line bus.

5. The method of claim 1 wherein the impedance interconnect is a microstrip transmission line bus.

6. The method of claim 1 wherein the first bus includes a plurality of traces exhibiting a first width and the interconnect includes a plurality of traces exhibiting a width greater than the width of the traces of the first bus.

7. The method of claim 1 wherein the first bus is a PCI bus.

8. The method of claim 1 wherein the first bus is a PCI-X bus.

9. The method of claim 1 wherein the first and second connectors are closely spaced within a 1U dimension.

10. The method of claim 1 wherein the riser card is oriented substantially perpendicular with the board on which the first bus is situated.

11. The method of claim 2 wherein the riser card is oriented substantially perpendicular with the board on which the first bus is situated and the expansion card is situated substantially parallel with the board on which the first bus is situated.

12. An information handling system (IHS) comprising:

a motherboard including a processor;

a port situated on the motherboard and coupled to the processor;

a first connector situated on the motherboard and coupled to the port by a first bus therebetween, the first bus exhibiting a bus impedance, the first connector exhibiting a connector impedance greater than the bus impedance;

and

a riser card situated in the first connector, the riser card including a second connector and an interconnect between the second connector and the first connector, the second connector exhibiting a connector impedance approximately equal to the connector impedance of the first connector, the impedance of the interconnect being sufficiently low to compensate the amount by which the connector impedance exceeds the bus impedance.

13. The IHS of claim 12 including an expansion card situated in the second connector of the riser card, the expansion card including a second bus exhibiting a bus impedance approximately equal to the impedance of the first bus, the impedance of the interconnect being sufficiently low that the aggregate impedance of the first connector, the interconnect and the second connector is approximately the same as the first impedance.

14. The IHS of claim 12 wherein the first bus is a microstrip transmission line bus.

15. The IHS of claim 12 wherein the interconnect is a microstrip transmission line bus.

16. The IHS of claim 12 wherein the first bus includes a plurality of traces exhibiting a first width and the interconnect includes a plurality of traces exhibiting a width greater than the first width.

17. The IHS of claim 12 wherein the first bus is a PCI bus.

18. The IHS of claim 12 wherein the first bus is a PCI-X bus.

19. The IHS of claim 12 wherein the first and second connectors are closely spaced within a 1U dimension.

20. The IHS of claim 12 wherein the riser card is oriented substantially perpendicular with the motherboard on which the first bus is situated.

21. The IHS of claim 13 wherein the riser card is oriented substantially perpendicular with the motherboard on which the first bus is situated and the expansion card is situated substantially parallel with the motherboard on which the first bus is situated.